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EXAMINER

LEE, EUGENE

ART UNIT

PAPER NUMBER

2815

DATE MAILED: 01/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

10/039,439

Applicant(s)

RABADAM ET AL.

Examiner

Eugene Lee

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 01 November 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-11 and 13-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-11 and 13-20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 11/1/04.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## DETAILED ACTION

### *Specification*

1. The amendment filed 5/17/04 is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure. 35 U.S.C. 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: the charge pump circuit **to provide a programming voltage potential to the memory array**.

Applicant is required to cancel the new matter in the reply to this Office Action.

### *Claim Rejections - 35 USC § 112*

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1 thru 11, and 18 thru 20 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The specification does not describe the charge pump circuit **to provide a programming voltage potential to the memory array** (claims 1, and 18).

*Claim Rejections - 35 USC § 103*

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1, 6, 13, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Humphrey et al. 6,476,486 B1 in view of Mart et al. 5,563,838 in view of Merritt et al. 6,490,220 B1. Humphrey discloses (see, for example, Fig. 8) an integrated circuit mounting package comprising an integrated circuit die 20 and electronic device 37. The electronic device is connected to the integrated circuit die by a contact pad 21. In column 2, lines 34-43, Humphrey discloses the electronic device may be any passive or active device or **another electronic device**. Humphrey does not specifically state the integrated circuit die including a memory array. However, it was extremely well known in the art at the time of invention that integrated circuit dies include memory arrays. Mart teaches (see, for example, column 1, lines 28-39) that integrated circuit chips come in a variety of forms, i.e. DRAM, SRAM, ROM, gate arrays, etc., which are all types of memory chips. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to have a memory array in order to form a memory device, and since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Humphrey in view of Mart does not disclose a charge pump circuit. However, Merritt discloses (see, for example, FIG. 11) an IC chip 900 comprising a PLL circuit (charge pump). In

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column 9, lines 33-48, Yao discloses the PLL circuit as a charge pump. The charge pump is used for a clock signal. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to have a charge pump circuit in order to generate a clock signal for a memory array.

6. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Futatsuya et al. 5,999,475 in view of Mart et al. 5,563,838. Futatsuya discloses (see, for example, column 4, lines 50-55) a memory device comprising a chip (integrated circuit die), and a charge pump circuit. The charge pump circuit is mounted on the chip for the purpose of generating various voltages. Futatsuya does not disclose a memory array. However, it was extremely well known in the art at the time of invention that integrated circuit dies include memory arrays. Mart teaches (see, for example, column 1, lines 28-39) that integrated circuit chips come in a variety of forms, i.e. DRAM, SRAM, ROM, gate arrays, etc., which are all types of memory chips. These forms are arrays that store data in an easy-to-access way. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to have a memory array in order to form a memory device that stores data in an easy-to-access way.

7. Claims 2 thru 4, 7 thru 10, and 14 thru 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Humphrey et al. '486 B1 in view of Mart et al. '838 in view of Yao '204 as applied to claims 1, 6, 13, 18 and 19, and further in view of Spielberger 6,005,778. Humphrey in view of Mart in view of Yao does not disclose the passive component being mounted to the integrated circuit die with an epoxy material. However, Spielberger states (see, for example,

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column 4, lines 40-42 and column 4, lines 12-17) that a chip is bonded by a conductive or nonconductive adhesive, and that epoxies are an example of adhesives. It would have been obvious to one of ordinary skill in the art at the time of invention to use an epoxy material in order to stabilize the passive component on the integrated circuit die.

Regarding claim 3, Humphrey in view of Mart in view of Yao in view of Spielberger discloses the claimed invention except for the epoxy material between the passive component and the integrated circuit die being less than about 0.050 millimeters in thickness. However, it was well known in the art at the time of invention to use this thickness in order to reliably attach one semiconductor component to another component in a semiconductor device. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to use an epoxy material being less than about 0.050 millimeters in thickness, in order to reliably attach the chip to another electronic device, and since it has been held that discovering an optimum value of a result effective value involves only routine skill in the art. In re Boesch, 617 F. 2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claims 8-10, Humphrey in view of Mart in view of Yao does not disclose wires to connect the integrated circuit or passive component to the substrate. However, Spielberger discloses (see, for example, left side of Figure 5) wires (first wire bond) 28a that connect the integrated circuit 40b to substrate 14b. For claims 9 and 10, Spielberger discloses (see, for example, right side of Figure 5) other wires (second wire bond) 28a that connect the passive component to the substrate. It would have been obvious to one of ordinary skill in the art at the time of invention to include these wires in order to make a reliable connection between the integrated circuit or passive component to the substrate.

8. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Humphrey et al. '486 B1 in view of Mart et al. '838 in view of Yao '204 as applied to claims 1, 6, 13, 18 and 19 above, and further in view of Manning et al. '5,962,887. Humphrey in view of Mart in view of Yao does not disclose the passive component including a capacitor or an inductor. However, Manning discloses (see, for example, column 1, lines 29-31) that charge pump circuits having capacitors that convert an input power supply voltage to an output power supply of different voltage or polarity. In column 6, lines 31-35, Manning further discloses the capacitor in a charge pump circuit that lessens the power supply voltage. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to have the passive component including a capacitor or an inductor in order to form a charge pump that can convert an input power supply voltage to an output power supply of different voltage or polarity, and/or lessen the power supply voltage.

9. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Humphrey et al. '486 B1 in view of Mart et al. '838 in view of Yao '204 as applied to claims 1, 6, 13, 18 and 19, and further in view of Javanifard et al. 6,385,033 B1. Humphrey in view of Mart in view of Yao does not disclose the integrated circuit die including a flash memory array. However, it was very well known in the art that flash memory arrays were one of many types of memory arrays utilized in memory chips. Javanifard discloses (see, for example, column 6, lines 9-15) a memory circuit device comprising a flash memory. Therefore, it would have been obvious to

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one of ordinary skill in the art at the time of invention to use a flash memory in order to utilize a common memory array that capably reads, writes, and stores data in a semiconductor device.

10. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Humphrey et al. '486 B1 in view of Mart et al. '838 in view of Yao '204 as applied to claims 1, 6, 13, 18 and 19, and further in view of Sundstrom 5,864,177. Humphrey in view of Mart in view of Yao does not disclose a wire bond to electrically couple at least one passive component and the integrated circuit. However, it was well known in the art at the time of invention to use wires to connect components of a semiconductor device. Sundstrom teaches (see, for example, FIG. 3) a semiconductor device comprising a passive device 12 and an underlying die 10. A bonding wire 28 couples the passive device to the die 10. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to use a bonding wire in order to reliably couple the voltage regulator and chip together.

### *Response to Arguments*

11. Applicant's arguments filed 11/1/04 have been fully considered but they are not persuasive.

Regarding the specification objection and 112 rejection that the limitation "the charge pump circuit **to provide a programming voltage potential to the memory array**" is not new matter, this argument is not persuasive. The limitation "to provide a programming voltage potential" is supported (see, page 4, lines 16-18) by the applicant's disclosure in regards to a voltage regulator, however, the disclosure does not support the same limitation for a charge



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pump circuit. Nowhere in the disclosure does the applicant state that the charge pump circuit providing a programming voltage potential to the memory array.

Regarding the applicant's argument on page 9 of the response filed 11/1/04 that the Office action has not established a prima facie case of obviousness, this argument is not persuasive. The rejection of claims 1-11, and 13-20 is based on the combination of Humphrey in view of Mart in view of Yao, not only Humphrey in view of Yao. Humphrey in view of Mart discloses an integrated circuit with a memory array. Memory arrays possess clock signals for reading the inputs and writing the outputs in an orderly fashion. Therefore, a prima facie case of obviousness has been established in that it would have been obvious to have a charge pump in the memory device of Humphrey in view of Mart in order to generate a clock signal.

### *Conclusion*

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.


### **INFORMATION ON HOW TO CONTACT THE USPTO**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Lee whose telephone number is 571-272-1733. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Eugene Lee  
January 24, 2005

  
**GEORGE ECKERT**  
**PRIMARY EXAMINER**